REMARKS

In the instant application, Claims 1-24 are rejected under 35 U.S.C. § 103(a). The Applicants hereby traverse the outstanding rejections, and request reconsideration and withdrawal in light of the remarks contained herein. Claims 1-24 are pending in this application.

Claims 1-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ginetti et al., US Patent No. 6,170,080 (hereinafter *Ginetti*)) in view of Jones et al., US Patent No. 5,629,860 (hereinafter *Jones*). To establish a prima facie case of obviousness, three basic criteria must be met, see M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined must teach or suggest all the claim limitations. Without conceding the first or second criteria, Applicant respectfully asserts that the cited references do not suggest or teach all the claim limitations.

Claim 1 includes "building a model of said signal routes including resistance and capacitance values," as a limitation. In the Office Action, the Examiner concedes that *Ginetti* does not teach building a model that includes the resistance value, and relies on *Jones* to teach this element, see Office Action page 3. However, the Applicants respectfully assert that *Jones* does not build a model that includes a resistance value. As column 8 lines 40-50 states, the method taught by *Jones* "requires as input only the capacitive load, C_1, for back annotation of routing delays." *Jones* does indicate that the resistance should be taken into account in the circuit estimation, however, instead of determining a value for the resistance and building a model that includes it, *Jones* merely adjusts the recorded capacitance value to compensate. Because the cited references do not teach or suggest the claim limitations, the Applicants respectfully assert that the Examiner withdraw the 35 U.S.C. § 103(a) rejection of record for claim 1.

Claims 2-10 depend directly from base claim 1, and thus inherit all its limitations. Thus, each of the claims 2-10 sets forth features and limitations not recited by the

combination of *Ginetti* and *Jones*, and the Applicants respectfully assert that they are patentable over the 35 U.S.C. § 103(a) rejection of record.

Claim 11 includes "building a model of said signal routes including resistance and capacitance values," as a limitation. In the Office Action, the Examiner concedes that *Ginetti* does not teach building a model that includes the resistance value, and relies on *Jones* to teach this element, see Office Action page 3. However, the Applicants respectfully assert that *Jones* does not build a model that includes a resistance value. As column 8 lines 40-50 states, the method taught by *Jones* "requires as input only the capacitive load, C_1, for back annotation of routing delays." *Jones* does indicate that the resistance should be taken into account in the circuit estimation, however, instead of determining a value for the resistance and building a model that includes it, *Jones* merely adjusts the recorded capacitance value to compensate. Because the cited references do not teach or suggest the claim limitations, the Applicants respectfully assert that the Examiner withdraw the 35 U.S.C. § 103(a) rejection of record for claim 11.

Claims 12-20 depend directly from base claim 11, and thus inherit all its limitations. Thus, each of the claims 12-20 sets forth features and limitations not recited by the combination of *Ginetti* and *Jones*, and the Applicants respectfully assert that they are patentable over the 35 U.S.C. § 103(a) rejection of record.

Claim 21 includes "means for building a model of said signal routes including resistance and capacitance values," as a limitation. The Examiner concedes that *Ginetti* does not teach building a model that includes the resistance value, and relies on *Jones* teach this element, see Office Action page 3. However, the Applicants respectfully assert that *Jones* include a means that builds a model that has a resistance value. As column 8 lines 40-50 states, the system taught by *Jones* "requires as input only the capacitive load, C_1, for back annotation of routing delays." *Jones* does indicate that the resistance should be taken into account in the circuit estimation, however, instead of determining a value for the resistance and building a model that includes it, *Jones* merely adjusts the recorded capacitance value to compensate. Because the cited references do not teach or suggest the claim limitations, the Applicants respectfully assert that the Examiner withdraw the 35 U.S.C. § 103(a) rejection of record for claim 21.

Claims 22-24 depend directly from base claim 1, and thus inherit all its limitations. Thus, each of the claims 22-24 sets forth features and limitations not recited by the combination of *Ginetti* and *Jones*, and the Applicants respectfully assert that they are patentable over the 35 U.S.C. § 103(a) rejection of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV256033654US, in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Date of Deposit: August 20, 2003

Typed Name: John Pallivathukal

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Respectfully submitted,
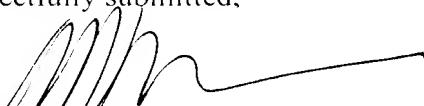
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